Ending in Fall 2024, I completed my Creative Component graduate research with Dr. Henry Duwe at Iowa State University, partnered with Gregory Ling. As part of my work, I had the opportunity to continue working on open-source ASIC design, utilizing the same open-source process supported by eFabless on the SkyWater 130nm technology. As part of my work, I helped document the digital and analog ASIC design flows required by eFabless to generate tapeout ready submissions. Additionally, I provided tutorials and guides on how to step through simple design for both design flows. In terms of deliverables, I was expected to submit an approved research paper to Iowa State University’s digital library, as well as a 45-minute oral exam to my major professor, Dr. Duwe. Attached are both the presentation and paper that I submitted for my final deliverables. By the end of our research, we were able to successfully establish Iowa State’s first ASIC design club, ChipForge, and provide them with all the necessary tools to create a tapeout ready design.